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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,796	06/08/2000	Gordon J. Vreugdenhil	1467-14	9846

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SILCON VALLEY PATENT GROUP LLP
2350 MISSION COLLEGE BOULEVARD
SUITE 360
SANTA CLARA, CA 95054

EXAMINER	
SHARON, AYAL I	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,796	VREUGDENHIL ET AL.	
	Examiner	Art Unit	
	Ayal I Sharon	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Introduction

1. Claims 1-23 of U.S. Application 09/590,796 filed on 06/08/2000 are presented for examination. Paper #9 (filed 11/7/03) amends the specification but does not amend, add, or cancel any claims.
2. The previous rejections based on prior art have been withdrawn, and new rejections have been applied. This action is Non-Final.

Claim Interpretations

3. At one place in the Specification (p.4, lines 1-3), Applicants define the term "**slot**" in terms of a "each system variable is said to have a slot", as follows (Emphasis added):

> "In a system of simultaneous equations, each system variable is said to have a "slot" and there is some set of equations that can be used to fill the slot in order to associate the system variable with an equation for solving the system of equations."

At another place in the Specification (p.2, lines 10-15), Applicants use the term "**slot**" interchangeably with system variables (Emphasis added):

> "The simulator assembles a system of simultaneous equations. Equations that do not change depending on the circumstances are permanently associated with a system variable or slot. The conditions that apply to the conditional equations are evaluated. A conditional equation is active when the conditions related to the conditional equation evaluate to true. The active conditional equations are then assigned to slots in the system of

> simultaneous equations, which can then be solved to determine the values of the system variables."

It is therefore not clear what constitutes a "**slot**". Examiner therefore interprets "slot" as being interchangeable with "system variable".

4. Examiner interprets the functionality of "simultaneous equations" as being equivalent to the "simultaneous statements" functionality taught in IEEE Standard 1076.1-1999. March 18, 1999. (See IEEE Std 1076.1-1999, pp.225, Section "15. Simultaneous Statements").

5. Applicants define the term "**analog solution iteration**" as follows (See Specification, p.4, lines 21-23):

> "An analog solution iteration is defined to occur when the analog solver requires that values need to be determined for the expressions forming the equations in the system."

6. Applicants define the term "**dynamic slot target variable**" as follows (See Specification, p.5, lines 7, and 11-14):

> "Assume that the partitioning results in a set of system variables $Q_1 \ldots Q_m$ and ... For each *j* from 1 to *m*, generate a new unconditional association between the slot for [system variable] Q_j and a variable q'_j where q'_j is a new temporary variable that is otherwise undefined. Each q'_j is called the ***dynamic slot target*** variable for the associated [system variable] Q_j."

7. Examiner interprets the term "conditional equation" in the following limitation of Claim 1 as being the "active conditional equation", just like its antecedent (Emphasis Added):

> assigning a value for the active conditional equation to a dynamic slot target variable at the current analog solution iteration, thereby associating the **[active]** conditional equation with a slot in the system of simultaneous equations;

This is in order to preserve the reference to the antecedent.

8. Claim 12 is being interpreted as reading as follows: "A computer-readable medium containing a program, that when executed, implements a method for solving a system of equations". While Examiner is not requiring the Applicants to amend the claim, it is recommended in order to eliminate any potential issues of operability under 35 U.S.C. 101.

Specification

9. The disclosure is objected to because of the following informalities: page 3 of the specification has blank lines associated with the U.S. Patent Application Serial Number and the filing date of a specific application. Appropriate correction is required.

Double Patenting

10. Claims 1, 12, and 22 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 18 of U.S. Patent No. 6,532,569. Although the conflicting claims are not identical, they are not patentably distinct from each other because the cited claims in the application claim "selecting an active conditional equation" or "selecting a set of active conditional equations", while the cited claim in the issued patent claims "... classify an unclassified variable as an intermediate variable if the unclassified variable is defined by an equation ...". All dependent claims inherit this defect.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 1, 2, 12, and 22 all claim the limitation "solving the system of simultaneous equations". All dependent claims inherit this defect.

The Applicants have expressly stated in the Specification (p.6, lines 8-9) that:

> "How the system of simultaneous equations is solved is known in the art, and will not be further described here."

Examiner notes that the fields of integer programming and linear programming include many non-trivial problems and many problems with no solution. Moreover, no references have been incorporated by reference into the specification, yet this functionality is claimed, and is critical to the functioning of the invention. This rejection has been maintained.

14. Claims 22-23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to

enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The element "translation software" has not been enabled in the specification. The specification (p.8, lines 10-12) says that

> "Translation software 435 translates a hardware description language of a physical circuit or system, such as [an] HDL file 455, into the systems of equations."

It is not clear if this "translation" is equivalent to compilation, parsing, or some other sort of transformation of the original HDL code. The details of how the transformation takes place, and what is the form of the final product (the "systems of equations") is missing from the disclosure. Given the large number of possible solutions, it would require one of ordinary skill in the art undue experimentation to arrive at the desired result.

15. Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: the preamble refers to "In a computer simulation of a physical circuit or system ...", however, none of the claimed limitations make reference to simulation. Instead, the final limitation makes reference to "... using the solution to the system of simultaneous equations to validate the physical circuit or system." However, no mention is made as to how the solution is used to validate the system.

16. Claims 2-23 rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap

between the elements. See MPEP § 2172.01. The omitted elements in Claims 2, 12, and 22 are: the final step(s) after solving the system of simultaneous equations at the current iteration. The term "current iteration" implies that there are additional iterations. It is not clear when and how the final iteration is reached, nor what happens once the final iteration is reached.

Claim Rejections - 35 USC § 101

17. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

18. Claims 1-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are not concrete or tangible because the claimed invention does not provide a concrete and tangible result, only the broad "solution to the system of simultaneous equations." By comparison, the example "useful, concrete, tangible results" cited in MPEP §2106 (II)(A), include telephone billing data, share price data, and pixel illumination intensity. The claims in the current application only refer to a general "solution".

19. Claims 2-23 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The claims are not useful, because a specific utility is lacking. Unlike Claim 1, which claims "... using the solution ... to validate the physical circuit or system", no utility is given for "... solving the

system of simultaneous equations ..." in Claims 2, 12, or 23. Once the system of equations is solved, it is not clear what useful benefit is derived from the solution.

20. In regards to Claims 12-21, please note the Examiner's related comment in paragraph #7 of this Office Action.

Response to Arguments

Re: Claim Rejections - 35 USC § 112

21. Applicants persuasively argue (paper #9, p.5, lines 1-21) that "selection software" and "selecting an active conditional equation" are enabled in the specification. This rejection has been withdrawn.

22. Applicants persuasively argue (paper #9, p.5, line 27 to p.6, line 10) that "assignment software" and "assigning a value for the active conditional equation to a dynamic slot target variable" are enabled in the specification. This rejection has been withdrawn.

23. Applicants unpersuasively argue (paper #9, p.5, line 27 to p.6, line 10) that "solution software" and "solving the system of simultaneous equations" are well known in the art. Examiner notes that the fields of integer programming and linear programming include many non-trivial problems and many problems with no solution. The Applicants have expressly stated in the Specification (p.6, lines 8-9) that:

> "How the system of simultaneous equations is solved is known in the art, and will not be further described here."

Moreover, no references have been incorporated by reference, yet this functionality is claimed, and is critical to the functioning of the invention. This rejection has been maintained.

24. Applicants unpersuasively argue (paper #9, p.7, lines 9-13) that "translation software" in Claims 22-23 are enabled because U.S. Patent 6,532,569 was granted to the Applicants with a similar disclosure. Examiner is not permitted to comment on the validity of an issued patent. Therefore the Examiner cannot use this argument as sufficient reason for withdrawing the rejection. This rejection has been maintained.

Re: Claim Rejections - 35 USC § 102

25. In light of the teaching of the Sasaki reference "A New Dynamic Equation Scheduling to Extend VHDL-AMS", which is described in greater detail in the "Conclusion" section of this Office Action, all of the 35 U.S.C. 102 rejections based on the IEEE Std. 1076.1-1999 have been withdrawn.

Conclusion

26. The following prior art, made of record and not relied upon, is considered pertinent to applicant's disclosure.

27. Sasaki, Hisashi. "A New Dynamic Equation Scheduling to Extend VHDL-AMS". Proc. of Asia-Pacific Conf. on Chip Design Languages. (APCHDL '99). Fukuoka, Japan. Oct. 6-8, 1999. (Henceforth referred to as "**Sasaki**").

The Sasaki reference has a publication date (Oct. 6-8, 1999) that is after the priority date of the application (June 18, 1999). However, Examiner finds that it is pertinent to the application because of the following teaching found in the "Abstract" section of the reference:

> "This paper proposes an equation scheduling that manipulates analog equations dynamically. The conventional VHDL-AMS has no such capability."

This teaching confirms Applicants' argument (paper #9, p.10, lines 13-15) that "... neither a static assignment scheme nor a dynamic assignment scheme is disclosed in IEEE [Std. 1076.1-1999] ..."

As a consequence of this, Examiner has withdrawn all of the art rejections based on IEEE Std. 1076.1-1999 that were issued in the previous Office Action (paper #7).

As noted above, the Sasaki reference post-dates the priority filing date of this application. Examiner has not been able to find a reference that teaches dynamic scheduling of analog equations with IEEE Std. 1076.1-1999 (also called VHDL-AMS) and that also pre-dates the priority filing date of this application.

28. Frey, Peter et al. "SEAMS: Simulation Environment for VHDL-AMS". Proc. of the 30th Conf. on Winter Simulation. Washington DC.. Dec. 13-16, 1998. (Henceforth referred to as "**Frey**"). The Frey reference teaches (Section 6, p.543) the following:

> "VHDL-AMS enables the modeler to state arbitrary equations in the form of Equation 1. SPICE-like solvers support only a fixed set of equations. To support dynamic equation sets, some form of symbolic differentiation is required during elaboration, and the fixed set simulator must be

> augmented to form CE sets prior to the solution process. SEAMS takes advantage of an automatic differentiation package called ADOL-C (Griewank et al. 1996) to provide the time derivatives during runtime."

However, Frey does do expressly teach the use of "dynamic slot target variables", nor of an equivalent. Moreover, the article about ADOL-C ("ADOL-C: A Package for Automatic Differentiation of Algorithms Written in C/C++") does not teach these features either.

29. In addition, the following articles were reviewed by the Examiner, and were not found to teach the use of "dynamic slot target variables", nor of an equivalent:

    a. Sasaki, T. et al. "Semantic Analysis of VHDL-AMS by Attribute Grammar". Proc. of Forum on Design Languages (FDL '98). Sept.6-10, 1998.

    b. Kazmierski, T. "A Formal Description of VHDL-AMS Analogue Systems". Proc. of Design Automation and Test in Europe (DATE '98). Feb. 23-26, 1998.

    c. Acuna, E.L. et al. "Simulation Techniques for Mixed Analog/Digital Circuits". IEEE Journal of Solid-State Circuits. Vol.25, Issue 2. April 1990. pp.353-363.

    d. Acuna, E.L. et al. "iSPLICE3: A New Simulator for Mixed Analog/Digital Circuits". Proc. of the 1989 IEEE Custom Integrated Circuits Conf. May 15-18, 1989. pp.13.1/1-13.1/4.

    e. El Tahawy, H. et al. "VHD$_e$LDO: A New Mixed Mode Simulation". Proc. 1993 European Design Automation Conf. (1993 EURO-DAC). Sept. 20-24, 1993. pp.546-551.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (703) 306-0297. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on (703) 305-9704. Any response to this office action should be mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Hand-delivered responses should be brought to the following office:

4th floor receptionist's office
Crystal Park 2
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The fax phone number for the organization where this application or proceeding is assigned is:

All communications: (703) 872-9306

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, whose telephone number is: (703) 305-3900.

Ayal I. Sharon

Art Unit 2123

January 21, 2004